上海贝岭 SHANGHAI BELLING

BL8089

PMU with 2 Synchronous 6V 1.5A Bucks and 2 CMOS 6V 500mA LDOs

DESCRIPTION

The BL8089 is a power management unit (PMU), with 2 synchronous Bucks and 2 CMOS low-dropout regulators that delivers a maximum current of 1.5A for Buck's output and a maximum current of 0.5A for each individual LDO's output.

The synchronous buck is a high-efficiency monolithic synchronous buck regulator using a constant frequency, current mode architecture. The device is available in an adjustable version. Supply current with no load is 40uA and drops to <1uA in shutdown. The 2.5V to 6V input voltage range makes the BL8089 ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems. PWM/PFM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 1.5MHz, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

Each of the 2 LDOs is low-dropout regulator that delivers a maximum current of 0.5A individual output. Typical dropout voltage at 0.5A load current is 0.8V. They have excellent load and line transient response and good temperature characteristics, which can assure the stability of chip and power system. The output accuracy of each channel is set within 2% by trimming.

Typical LDO output voltage: VO1=1.2V, VO2=1.8V. Other fixed voltage can be provided in the range of 1.0V~4.5V every 0.1V step. It also can be customized on command. LDOs can also work under a wide input voltage ranging from 1.8V to 6V. They can provide foldback short-circuit protection and output current limit function.

BL8089 is available in lead (Pb)-free QFN3x3-16 (with exposed pad for heat dissipation) package.

FEATURES

BUCK

- High Efficiency : Up to 96%
- Capable of Delivering 1.5A
- 1.5MHz Switching Frequency
- No External Schottky Diode Needed
- Low dropout 100% Duty operation
- PFM Mode for High Efficiency in Light Load
- Over temperature Protected
- Low Quiescent Current: 40μA
- Short Circuit Protection
- Inrush Current Limit and Soft Start

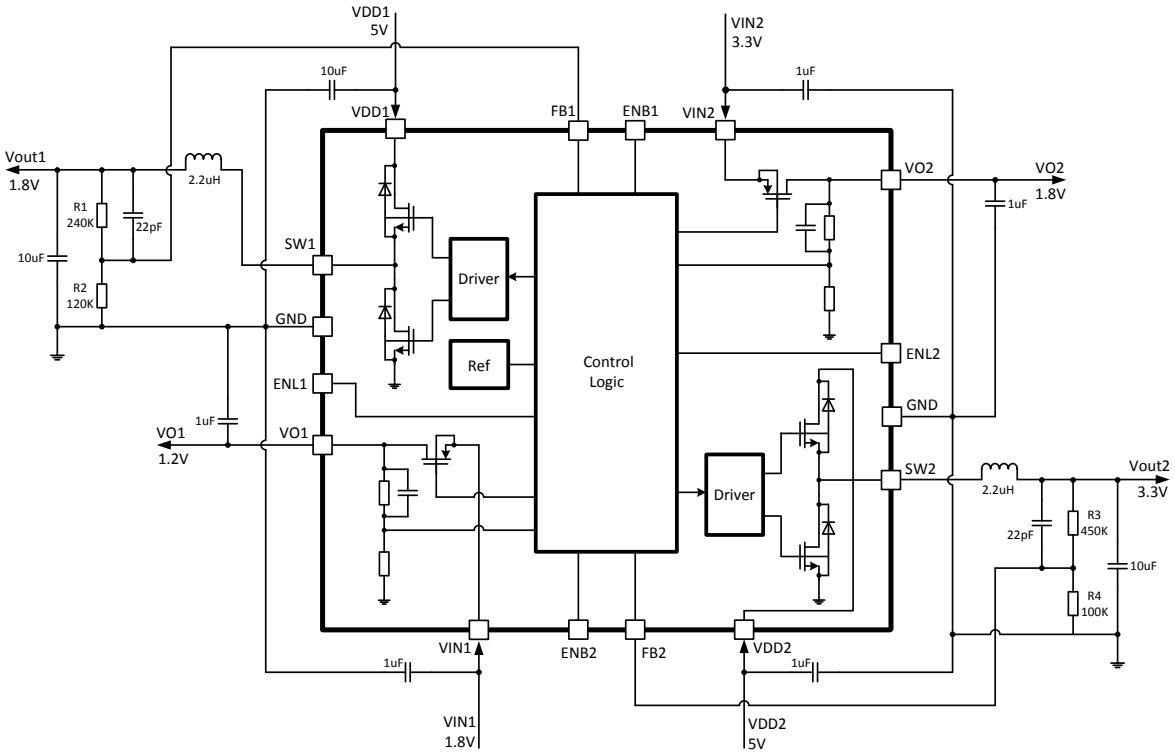
LDO

- Max output current for each channel is 0.5A
- Input voltage range: 1.8 – 6V
- Output voltage range: 1.0V~4.5V (customized on command every 0.1V step)
- Low power consumption: 50uA (Typ.)
- Low output noise (47uVRMS)
- Standby Mode: 0.1uA
- Low dropout voltage:
  600mV@I_{O1}=250mA, VO1=1.2V
  800mV@I_{O2}=500mA, VO2=1.8V
- High ripple rejection:65dB@1KHz (Typ.)
- Low temperature coefficient: ±100ppm/°C
- Excellent line regulation: 0.05%/V
- Highly accurate: ±2%
- Output current limit
- Fold-back short circuit current

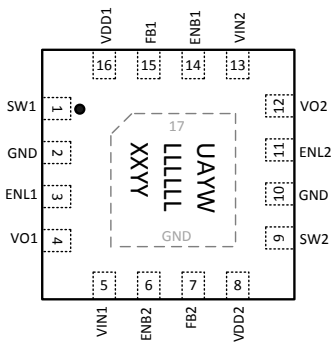
APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Wireless and DSL Modems
- Power source for cellular phones and various kind of PCSs
- Battery Powered equipment

TYPICAL APPLICATION



ORDERING INFORMATION

Mark Explanation		Ordering Information	
UA: Product Code YW: Date code(Year & Week) LLLLLL: Lot No. XX: Output Voltage(VO1) YY: Output Voltage(VO2)		QFN3x3-16 3000pcs/reel	BL8089CJKTR□□□□

ABSOLUTE MAXIMUM RATING

Parameter		Value
Max Input Voltage (VDD)		8V
Max Input Voltage (VIN)		8V
Max Operating Junction Temperature(Tj)		125°C
Ambient Temperature(Ta)		-40°C – 85°C
Maximum Power Dissipation	QFN3x3-16	2W
Package Thermal Resistance (θjc)		13°C / W
Package Thermal Resistance (θjA)		60°C / W
Storage Temperature(Ts)		-40°C - 150°C
Lead Temperature & Time		260°C, 10S

Note: *Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

RECOMMENDED WORK CONDITIONS

Parameter	Value
Input Voltage Range (VDD)	Max. 6V
Input Voltage Range (VIN)	Max. 6V
Operating Junction Temperature(Tj)	Max. 125°C

ELECTRICAL CHARACTERISTICS

(VDD=5V, VO1=1.2V, VO2=1.8V,T_A=25°C, unless otherwise stated)

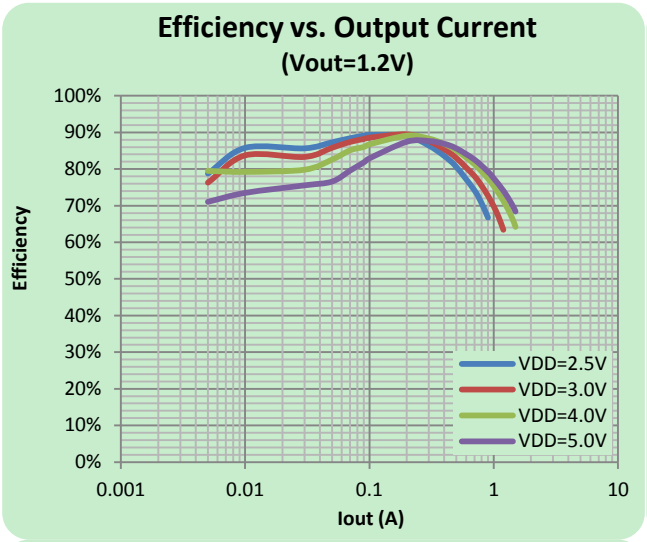
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUCK						
VDD	Input Voltage Range	BUCK1 or BUCK2	2.5		6	V
Vref	Feedback Voltage	VDD=5V	0.588	0.6	0.612	V
Ifb	Feedback Leakage current			0.1	1	uA
Iq	Quiescent Current	Active, Vfb=0.65, No Switching		40	70	uA
		Shutdown		0.1	1	uA
LnReg	Line Regulation	VDD=2.5V to 6V		0.1	0.2	%/V
LdReg	Load Regulation			0.5		%/A
Fsoc	Switching Frequency			1.5		MHz
RdsonP	PMOS Rdson	I_{SW}=100mA		300		mohm
RdsonN	NMOS Rdson	I_{SW}=-100mA		200		mohm
Ilimit	Peak Current Limit	VDD=5V, Vout=3.3V		2.2		A
Inoload*		VDD=5V, Vout=3.3V, Iout=0		43		uA
Iswlk	SW Leakage Current	V_{EN}=0V,VDD=Vsw=5V			1	uA
Ienlk	EN Leakage Current				1	uA
Vh_enb	EN Input High Voltage		1.05			V
Vl_enb	EN Input Low Voltage				0.95	V
LDO						
VIN	Input Voltage Range	LDO1 or LDO2	VO		6	V
Io (Max.)	Maximun Output Current	VIN-VO=1V	500			mA
VO1	Output Voltage	1mA≤Io1≤30mA , VIN1=1.8V	1.17	1.2	1.23	V
VO2	Output Voltage	1mA≤Io2≤30mA , VIN2=3.3V	1.774	1.8	1.836	V
LNR	Line Regulation	Io=40mA, 3V≤VIN≤6V		0.05	0.2	%/V
ΔVout	Load Regulation	VIN=VO+1V, 1mA≤Io≤0.5A		50	80	mV
Vdrop	Dropout Voltage	Io1=0.25A (VO1=1.2V)		0.5	0.6	V
		Io2=0.5A (VO2=1.8V)		0.75	0.9	V
Ilimit	Current Limit			1		A
Iss	Supply Current	VIN=VO+1V (LDO1 or LDO2)		50	120	uA
Rdischarge	Discharge Resistor	CE=0, Vout=3.0V		150		ohm
Vh_enl	ENL Input Voltage “H”		0.95		Vin	V
Vl_enl	ENL Input Voltage “L”		0		0.25	V
PSRR	Ripple Rejection	F=1KHz, Ripple=0.5Vp-p VIN=VO+1V		65		dB
ΔV/ΔT	Temperature coefficient			±100		ppm

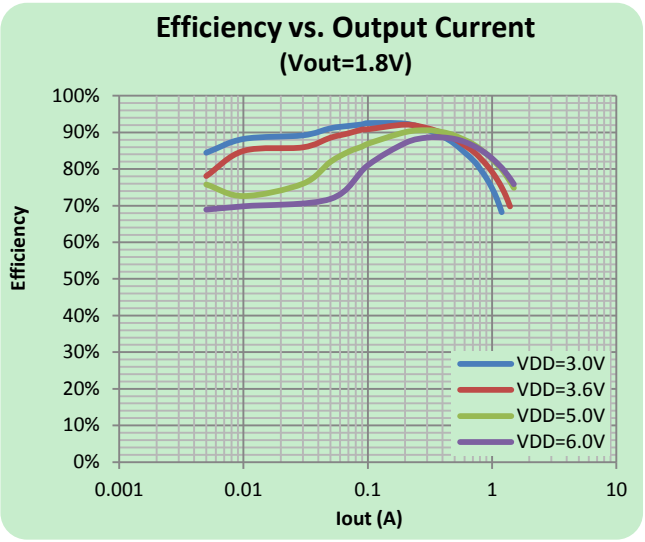
***Note:** * When Dutycycle >90%, Inoload will increase. e.g. VDD=3.5V/Vout=3.3V, Inoload=800uA.*

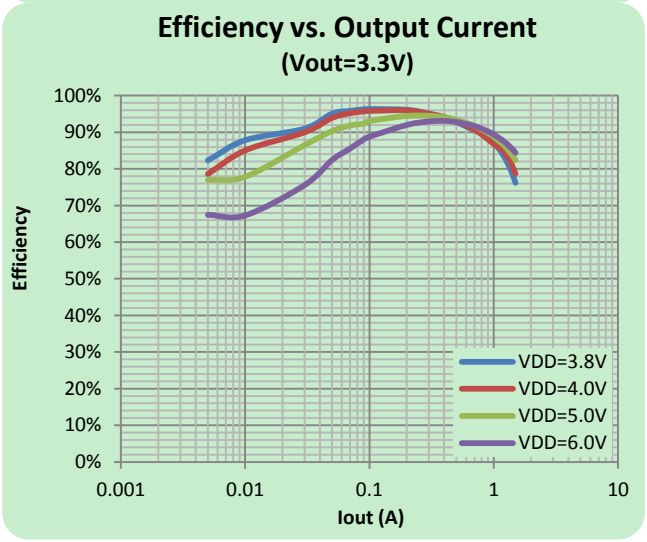
ELECTRICAL PERFORMANCE

Tested under TA=25°C, unless otherwise specified

BUCK



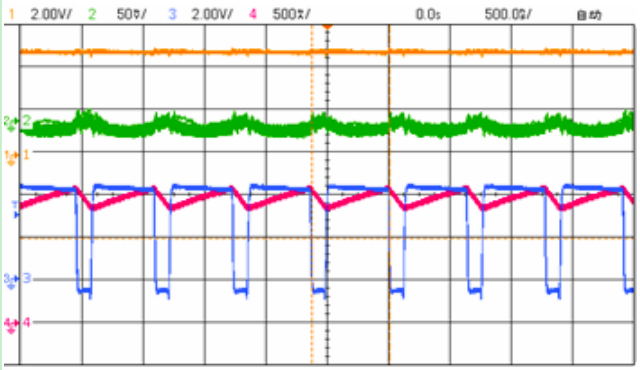




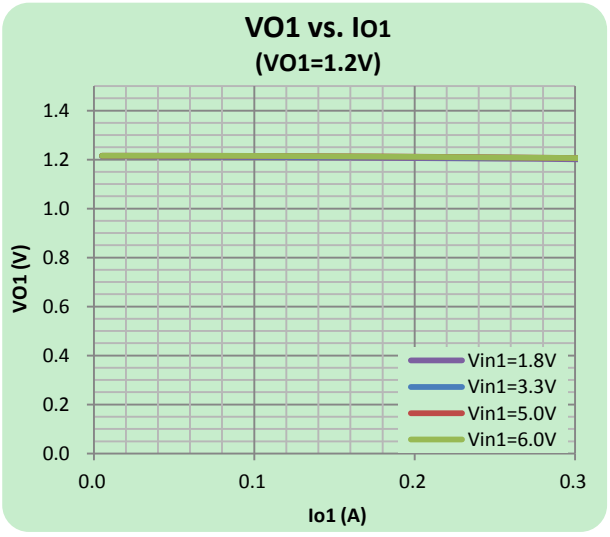
Output Ripple and SW at 1.5A load

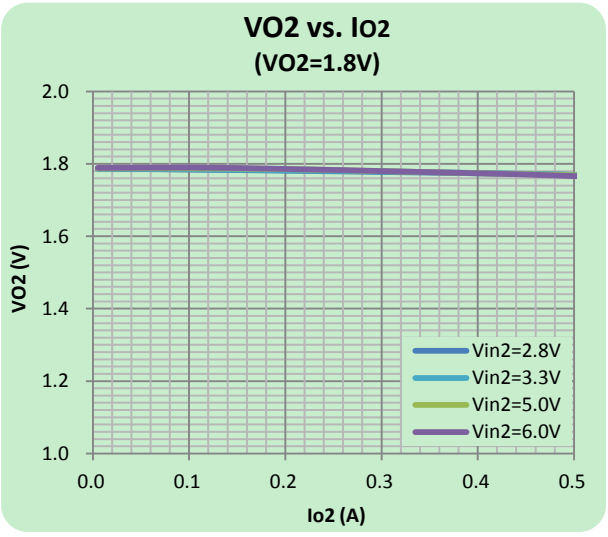
VDD=5V / Vout=3.3V

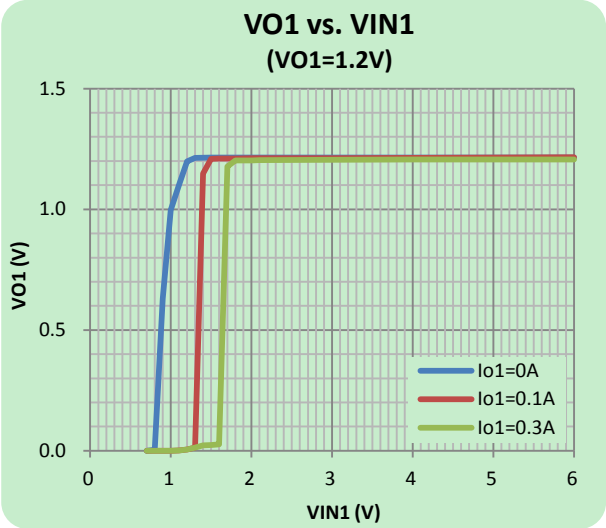
Ch1—VDD, Ch2—Vout, Ch3—Vsw, Ch4—I_L

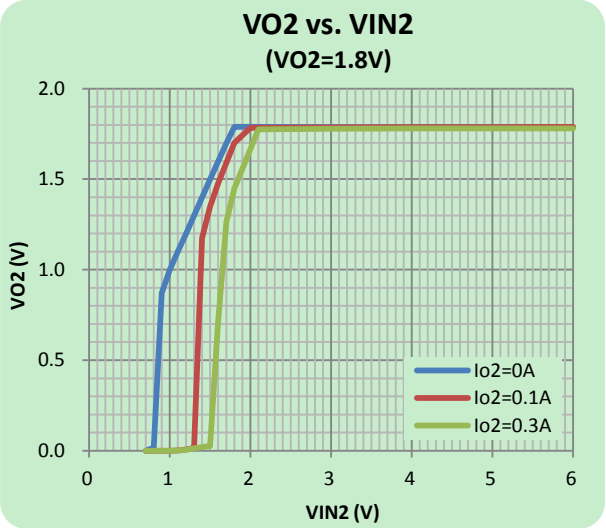


LDO









PIN DESCRIPTION

PIN #	NAME	DESCRIPTION	PIN #	NAME	DESCRIPTION
1	SW1	Switch Pin1	10	GND	Ground Pin
2	GND	Ground Pin	11	ENL2	LDO Enable Pin2
3	ENL1	LDO Enable Pin1	12	VO2	Output Pin2
4	VO1	Output Pin1	13	VIN2	Input Pin2
5	VIN1	Input Pin1	14	ENB1	BUCK Enable Pin1
6	ENB2	BUCK Enable Pin2	15	FB1	Feedback Pin1
7	FB2	Feedback Pin2	16	VDD1	Supply Voltage Input Pin1
8	VDD2	Supply Voltage Input Pin2	17	GND	Ground Pin (Thermal PAD)
9	SW2	Switch Pin2			

DETAILED DESCRIPTION

BUCK

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET of 2.2A(typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The buck utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to 2.2A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

The buck has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If VDD drops below 2.5V, the UVLO circuit inhibits switching. Once VDD rises above 2.5V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +170°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Setting Output Voltages

Output voltages are set by external resistors. The FB_ threshold is 0.6V.

For BUCK1: R1 = R2[(VOUT / 0.6) - 1]

For BUCK2: R3 = R4[(VOUT / 0.6) - 1]

Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

VRIPPLE = IL(PEAK)[1 / (2π x fOSC x COUT)]

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:
VRIPPLE(ESR) = IL(PEAK) x ESR

LDO

The device has build-in modules including high accuracy voltage reference, error amplifier, current limit, power transistors and driver circuit. Current limit functions ensure reliability of device and power system.

The bandgap module provides stable reference voltage whose temperature coefficient is compensated by careful design considerations. The temperature coefficient is under 100 ppm/°C. It has excellent load and line transient response and good temperature characteristics, which can assure the stability of chip and power system. The accuracy of output voltage is guaranteed by trimming technique.

THERMAL CONSIDERATIONS

Thermal consideration has to be taken account into to ensure proper function of the device. Power dissipation of BL8089 can be calculated as

LDO1 Power Dissipation = (VIN1-VO1)×IO1

LDO2 Power Dissipation = (VIN2-VO2)×IO2

BUCK1 Power Dissipation = VDD1×IDD1×10%

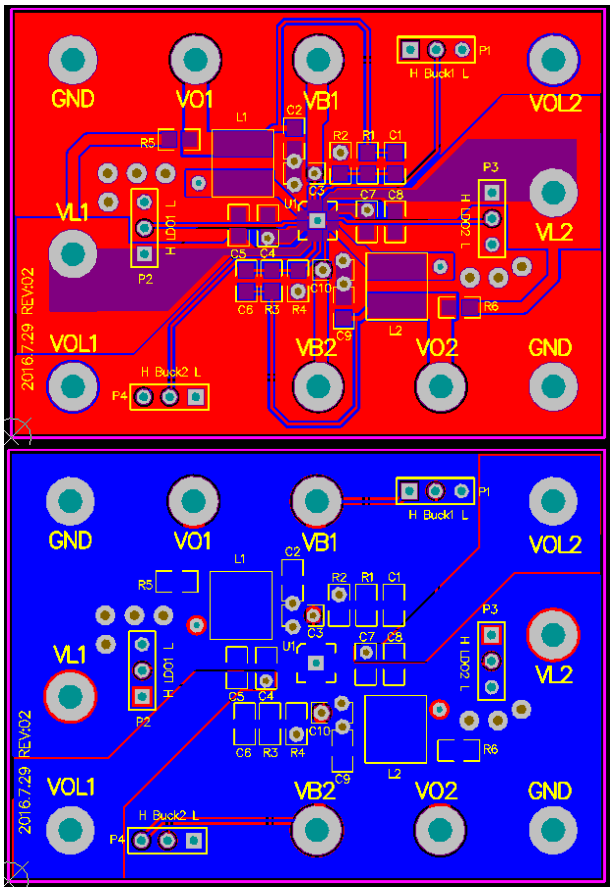
BUCK2 Power Dissipation = VDD2×IDD2×10%

Total Power Dissipation = LDO1 Power Dissipation + LDO2 Power Dissipation + BUCK1 Power Dissipation + BUCK2 Power Dissipation

For proper function and safe operation of the device, LDO1 power dissipation is recommended to be limited within 1W, LDO2 power dissipation is recommended to be limited within 1W, and total power dissipation is recommended to be limited within 2W.

APPLICATION INFORMATION

Layout is critical to achieve clean and stable operation. The switching power stage and heat dissipation requires particular attention. Follow these guidelines for good PC board layout:



1) Place decoupling capacitors as close to the IC as possible
2) Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current

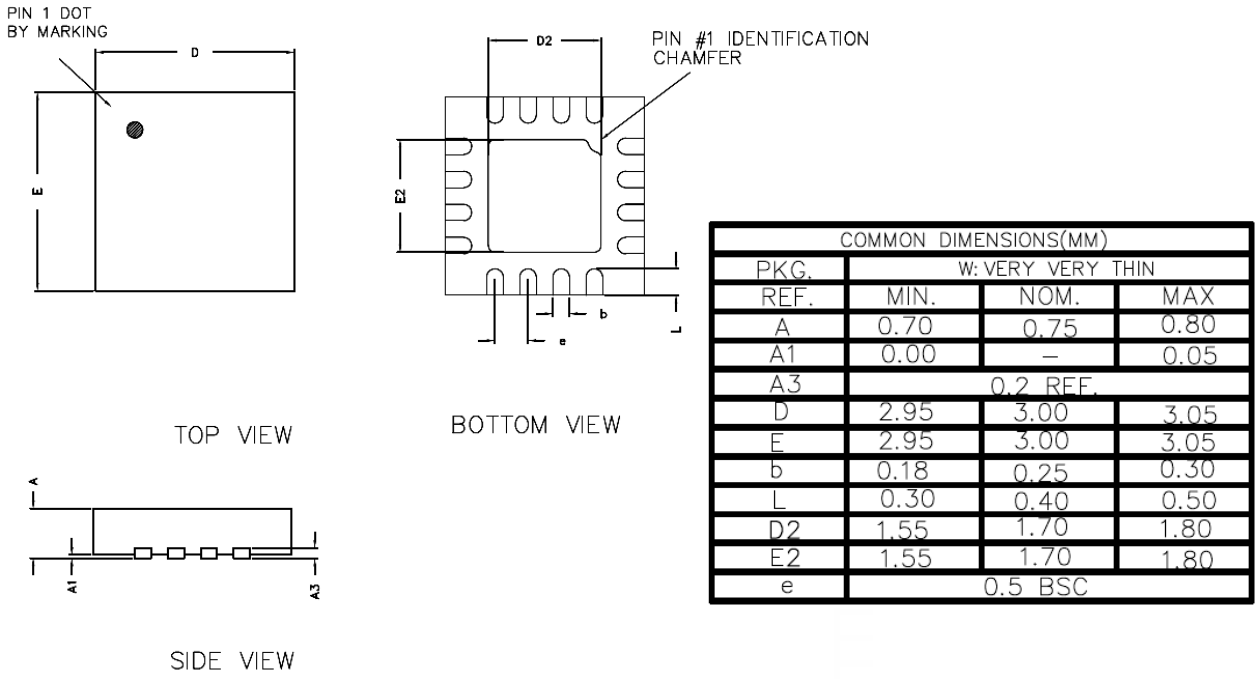
(CIN to VDD and CIN to GND) short. Avoid vias in the switching paths.

4) If possible, connect VIN, VO, VDD, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas.

PACKAGE OUTLINE

Package	QFN3x3-16	Devices per reel	3000	Unit	mm

Package specification：



COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.2 REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.18	0.25	0.30
L	0.30	0.40	0.50
D2	1.55	1.70	1.80
E2	1.55	1.70	1.80
e	0.5 BSC		